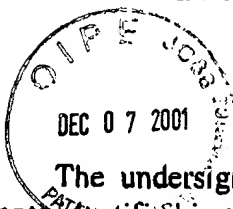


## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

POWER OF ATTORNEY BY ASSIGNEERECEIVED  
DEC 11 2001  
Technology Center 2000

The undersigned assignee of the entire interest in the patent applications and issued patents identified in the attached Exhibit A, by virtue of that certain assignment agreement dated November 27, 2000 by and among BAE Systems Information and Electronic Systems Integration, Inc. and Lockheed Martin Corporation, elects to conduct the prosecution of the patent applications and maintenance of the patents to the exclusion of the inventor(s) and earlier assignees.

The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following attorneys, all of Swidler Berlin Shereff Friedman, LLP, to prosecute the patent applications and maintain the patents listed in the attached Exhibit A and transact all business in the Patent and Trademark Office connected therewith:

Edward A. Pennington	32,588	John P. Moran	30,906
Michael A. Schwartz	40,161	Robert C. Bertin	41,488
Alicia A. Meros	44,937	Chadwick A. Jackson	46,495
Sean P. O'Hanlon	47,252	Eric J. Franklin	37,134

Please send all written communications to:

Edward A. Pennington  
Swidler, Berlin, Shereff, Friedman, L.L.P.  
3000 K Street, Washington, D.C. 20007  
Fax (202) 295-8478

Please direct all telephone calls to: Robert C. Bertin, 202-424-7872.

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**ASSIGNEE**

BAE SYSTEMS INFORMATION AND  
ELECTRONIC SYSTEMS INTEGRATION, INC.

Date:

*November 15, 2001*

By:

*Kevin M. Perkins*  
Kevin M. Perkins

Title: Vice President and Secretary-

Company General Counsel for its IEWS business

**EXHIBIT A**

<b>Title:</b>	<b>Application Number:</b>	<b>Filing Date:</b>	<b>Patent Number:</b>	<b>Issue Date:</b>
Error Detection And Fault Isolation For Lockstep Processor Systems	08/660640	07-Jun-1996	5,915,082	22-Jun-1999
Process To Personalize Master Slice Wafers And Fabricate High Density VLSI Components With A Single Masking Step	08/728880	10-Oct-1996	5,858,817	12-Jan-1999
Fault Tolerant MOSFET Driver	08/733080	16-Oct-1996	5,796,274	18-Aug-1998
Electrostatic Discharge Protection For Silicon-On-Insulator	08/812183	06-Mar-1997	6,034,399	07-Mar-2000
Ring Domains For Bandwidth Sharing	08/812184	06-Mar-1997	5,901,148	04-May-1999
Secure Data Transmission On A TDM Isochronous Network	08/837165	14-Apr-1997	5,970,095	19-Oct-1999
Digital Multi-Channel Demultiplexer/Multiplex (MCD/M Architecture)	08/884650	27-Jun-1997	5,867,479	02-Feb-1999
Control And Telemetry Signal Communication System For Geostationary Satellites	08/884675	27-Jun-1997	6,188,874B1	13-Feb-2001
Shallow Isolation Trench Forming Process For Silicon-On-Insulator Technology	08/987016	09-Dec-1997		
Reversible Keypad And Display For A Telephone Handset	08/989463	12-Dec-1997	6,052,606	18-Apr-2000
Integrated Circuit Package And Method Increasing Density Of I/O Leads	09/007980	16-Jan-1998		
Multi-Channel Overvoltage Protection Circuit	09/030902	26-Feb-1998	6,127,879	03-Oct-2000
Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture	09/241313	01-Feb-1999	6,091,704	18-Jul-2000
Error Detection And Fault Isolation For Lockstep Processor Systems	09/325641	04-Jun-1999	6,065,135	16-May-2000
Radiation Hardened Six Transistor Random Access Memory And Memory Device	09/325645	04-Jun-1999	6,111,780	29-Aug-2000
Satellite Telephone Handset	09/384429	27-Aug-1999		
Enhanced Single Event Upset Immune Latch Circuit	09/480454	11-Jan-2000	6,275,080	14-Aug-2001
In Situ Proximity Gap Monitor For Lithography	09/502062	10-Feb-2000		
Method And Apparatus For A Single Event Upset (SEU) Tolerant Clock Splitter	09/559659	28-Apr-2000		
Method And Apparatus For A Scannable Hybrid Flip Flop	09/559660	28-Apr-2000		
Method And Apparatus For A SEU Tolerant Clock Splitter	09/559661	28-Apr-2000		

Title:	Application Number:	Filing Date:	Patent Number:	Issue Date:
Distributed Determination Of Explicit Rate In An ATM Communication System	09/570050	12-May-2000		
Self-Equalized Low Power Precharge Sense Amp For High Speed SRAMs	09/570064	12-May-2000		
Tool Suite For The Rapid Development Of Advanced Standard Cell Libraries	09/597229	20-Jun-2000		
Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture	09/625641	25-Jul-2000		
Elimination Of Narrow Device Width Effects In Complementary Metal Oxide Semiconductor (CMOS) Devices	09/741028	21-Dec-2000		
Ball Grid Array (BGA) To Column Grid Array (CGA) Conversion Process	09/774010	31-Jan-2001		
Polyphase-Discrete Foulter Transform (DFT) Sub-band Definition Filtering Architecture	09/780348	12-Feb-2001		
Method And Apparatus For A Radiation Hardened Clock Splitter	09/838131	20-Apr-2001		

## PATENT ASSIGNMENT

THIS PATENT ASSIGNMENT is made and entered into as of the 27th day of November 2000, between Lockheed Martin Corporation, a Maryland corporation ("Assignor"), and BAE SYSTEMS INFORMATION AND ELECTRONIC SYSTEMS INTEGRATION INC. (formerly known as BAE SYSTEMS Sanders Inc.), a Delaware corporation ("Assignee").

### W I T N E S S E T H:

WHEREAS, Assignor is the owner of the entire right, title and interest in and to all of the patents and patent applications set forth on Schedule A annexed hereto and made a part hereof and has the unrestricted right to sell, assign and transfer such patents and patent applications; and

WHEREAS, pursuant to the terms of a Transaction Agreement, dated as of July 13, 2000, by and among Assignor, Assignee and BAE SYSTEMS North America Inc., a Delaware corporation, Assignor has agreed, among other things, to transfer to Assignee said patents and patent applications;

NOW, THEREFORE, in consideration of the sum of ten (\$10.00) dollars and other good and valuable consideration paid by Assignee to Assignor, the receipt and sufficiency of which is hereby acknowledged, Assignor hereby sells, assigns, transfers and sets over to Assignee, its successors and permitted assigns, Assignor's entire right, title and interest in and to the patents and patent applications set forth on Schedule A hereto, including (without limitation) all divisions, reissues, substitutions, continuations and extensions thereof, all priority rights under the International Convention for the Protection of Industrial Property for every member country (and any other international convention or treaty), any and all Letters Patent and reissues and extensions of Letters Patent granted thereon and any and all rights corresponding to any of the foregoing throughout the world and any and all accounts, contract rights, warranties, litigation claims and rights, including the right to sue for and collect upon all claims for profits and damages as a result of past infringement, if any, and other general intangibles of Assignor related to any of the foregoing, in each case whether now existing or hereafter acquired or created, whether owned, leased or licensed beneficially or of record and whether owned, leased or licensed individually, jointly or otherwise, together with the products and proceeds thereof (including license royalties and the proceeds of infringement suits), all payments and other distributions with respect thereto and any divisions, reissues, substitutions, continuations and extensions of any and all of the foregoing (all of the foregoing herein collectively referred to as the "Patents").

Assignor further agrees that it shall on the date hereof and from time to time thereafter, at the request of Assignee, perform or cause to be performed such acts and execute, acknowledge and deliver at the request of Assignee, such documents as may reasonably be required to evidence or effectuate the sale, conveyance, assignment, transfer and delivery to Assignee of the Patents or for the performance by Assignor of any of its obligations hereunder.

IN WITNESS WHEREOF, Assignor has executed this Patent Assignment as of the date above written.

LOCKHEED MARTIN CORPORATION

By: 

Name: Warren W. Lanning

Title: Director, Business Ventures

BAE SYSTEMS INFORMATION AND  
ELECTRONIC SYSTEMS INTEGRATION INC.

By: 

Name: Earl D. Munn

Title: Vice President

DISTRICT OF COLUMBIA ss.:

On the 27<sup>th</sup> day of November, 2000, before me personally came Warren W. Lanning, to me known (or satisfactorily proven), who being by me duly sworn, did depose and say that he is the Director, Business Ventures of Lockheed Martin Corporation, the corporation described in, and which executed the foregoing instrument, and that he was fully authorized to execute this Patent Assignment on behalf of said corporation.

Lisa A. Young  
Notary Public

My Comm. Expires \_\_\_\_\_

DISTRICT OF COLUMBIA ss.:

On the 27<sup>th</sup> day of November, 2000, before me personally came Frank P. Munns, to me known (or satisfactorily proven), who being by me duly sworn, did depose and say that he is the Vice President and Secretary of BAE SYSTEMS Information and Electronic Systems Integration Inc., the corporation described in, and which executed the foregoing instrument, and that he was fully authorized to execute this Patent Assignment on behalf of said corporation.

Lisa A. Young  
Notary Public

My Comm. Expires \_\_\_\_\_

SCHEDULE A

# LM Space Electronics & Communications

CaseNumber Title

FE-00003 High Density Integrated Circuit

Country Status File Date ApplNumb Issue Date PatNumber

US Expired 24-Jan-1979 5946 17-Jun-1980 4,208,079  
JP Abandone 20-Dec-1979 16487679 20-Jan-1984 1185552

FE-00006 Process for Increasing the Immunity of IC to Ionizing Radiation

FE-00007 FET Read Only Memory Cell With Work Line Augmented Precharging Of Bit Lines

US Secret 20-Jun-1982 393,012

JP Abandone 15-May-1984 09578784 10-Nov-1988 1464935  
GB Granted 24-Jul-1984 84108711.7 27-Sep-1989 0135699  
FR Granted 24-Jul-1984 84108711.7 27-Sep-1989 0135699  
AT Granted 24-Jul-1984 84108711.7 27-Sep-1989 0135699  
US Granted 20-Sep-1983 534,035 16-Feb-1988 4,725,986  
DE Granted 24-Jul-1984 84108711.7 27-Sep-1989 0135699  
EP Granted 24-Jul-1984 84108711.7 27-Sep-1989 0135699

FE-00008 Improved Local Oxide Isolation Process

US Secret 06-Jul-1984 643,902

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**CaseNumber Title**

FE-00009 High Density, High Performance, Single Event Upset Immune Data

Country	Status	File Date	ApplNumb	Issue Date	PatNumber
US	Granted	09-Mar-1987	23,426	10-Jan-1989	4,797,804
FR	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281,741
JP	Granted	20-Jan-1988	008597/88	07-Oct-1994	1878682
EP	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281,741
GB	Granted	22-Jan-1988	88100947.6	13-Jan-1993	281,741
DE	Granted	22-Jan-1988	88100947.6	13-Jan-1993	3877381308

FE-00010 Parity Generator Circuit And Method

EP	Pending	23-Jan-1989	89101069.6		
US	Granted	17-Feb-1990	156,026	07-Nov-1989	4,079,675
JP	Lapsed	10-Nov-1988	290385/88	14-Oct-1992	1703279

FE-00012 Soft Error Resistant CMOS Data Cells

US	Granted	31-Mar-1988	176,052	25-Jul-1989	4,852,060
GB	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	335,008
JP	Pending	20-Feb-1989	30541/89		
DE	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	3871945208
FR	Lapsed	23-Dec-1988	88121619.6	10-Jun-1992	355,008

FE-00016 Process for Increasing the Immunity of IC's to Ionizing Radiation

US	Secret	13-Sep-1988	246,136		
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**CaseNumber Title**

**FE-00017** Zero Standby Power, Radiation Hardened, Memory Redundancy Circuit

Country	Status	File Date	AppNumb	Issue Date	PatNumber
EP	Granted	03-May-1990	90108357.6	21-Aug-1996	419,760
DE	Granted	03-May-1990	90100357.6	21-Aug-1996	69028169.2
JP	Granted	07-Sep-1990	236022/90	17-Dec-1999	3015084
US	Granted	28-Sep-1989	414,889	26-Feb-1991	4,996,670
GB	Granted	03-May-1990	90108357.6	21-Aug-1996	419,760
FR	Granted	03-May-1990	90108357.6	21-Aug-1996	419,760
WO	Pending	09-Sep-1990	236022/90		

**FE-00020** A Method for improving gate oxide reliability of SOI in Mesa Type Transistors.

**FE-00021** CMOS Off Chip Driver for Fault Tolerant Cold Sparring

US	Secret	13-Jun-1990	544,140		
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**FE-00022** Method of Forming A frontside Contact to the Silicon Substrate of a SOI Wafer

EP	Granted	08-Oct-1991	91117104.9	28-Feb-1996	481,329
JP	Granted	11-Oct-1991	290475/91	08-Aug-1996	2549221
DE	Granted	08-Oct-1991	91117104.9	28-Feb-1996	69117420.2
FR	Granted	08-Oct-1991	91117104.9	28-Feb-1996	481,329
US	Granted	16-Oct-1990	598,300	26-May-1992	5,117,129
GB	Granted	08-Oct-1991	91117104.9	28-Feb-1996	481,329

**FE-00029** Small Cell Low Contact Assistance Rugged Power Field Effect Devices And Method Of Fabrication

JP	Granted	28-Mar-1994	057624/94	02-Dec-1996	2589952
US	Granted	03-Feb-1992	829,667	10-Aug-1993	5,234,851

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**CaseNumber Title****FE-00031** *Distributed Programmable Priority Arbitration***Country Status****File Date ApplNumb****Issue Date****PatNumber**

JP

Granted

01-Mar-1993

39810/93

27-Jun-1996

2531918

US

Granted

30-Apr-1992

876,239

26-Apr-1994

5,307,466

**FE-00035***Fast Fourier Transform Using Balanced Coefficients*

JP

Granted

22-Oct-1991

301336/91

13-Jun-1997

2662124

EP

Pending

13-Jun-1991

91109688.1

US

Granted

13-Jan-1993

004,217

15-Nov-1994

5,365,469

**FE-00040***An Electrostatic Discharge Protect Diode For Silicon-On-Insulator Technology*

JP

Granted

28-Mar-1994

6-57668/94

09-May-1997

2647339

DE

Granted

17-Feb-1994

94102415.0

21-Apr-1999

0622850

FR

Granted

17-Feb-1994

94102415.0

21-Apr-1999

0622850

EP

Granted

17-Feb-1994

94102415.0

21-Apr-1999

0622850

GB

Granted

17-Feb-1994

94102415.0

21-Apr-1999

0622850

US

Abandone

30-Apr-1993

056,042

**FE-00041***Method To Prevent Latch-Up And Improve Breakdown Voltage In SOI Mosfets*

EP

Pending

17-Feb-1994

94102414.3

18-Jun-1996

5,527,724

US

Granted

12-Sep-1994

304,639

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**CaseNumber Title**

FE-00042 *A Method Of Forming A Frontside Contact To the Silicon Substrate Of A SOI Wafer*

Country	Status	File Date	ApplNumb	Issue Date	PatNumber
US	Granted	30-Apr-1993	054,992	24-May-1994	5,314,841
DE	Pending	17-Feb-1994	94102416.8		
EP	Pending	17-Feb-1994	94102416.8		
JP	Granted	18-Apr-1994	078654/94	26-Feb-1999	2891321
GB	Pending	17-Feb-1994	94102416.8		
FR	Pending	17-Feb-1994	94102416.8		

FE-00052 *Power Bus Digital Communication System*

US	Granted	04-Oct-1993	131,346	01-Jul-1997	5,644,286
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FE-00057 *Single Even Upset Hardening Of Commercial VLSI Technology Without Circuit Redesign*

US	Pending	26-Oct-1993	141,505		
JP	Abandone	19-Oct-1994	6-253600		
EP	Pending	30-Aug-1994	94113502.2		

FE-00060 *Method To Radiation Harden The Buried Oxide In Silicon-On-Insulator Structures*

US	Granted	28-Oct-1993	142,030	01-Nov-1994	5,360,752
EP	Granted	14-Oct-1994	94116233.1	22-Dec-1999	652591A1

FE-00069 *Spure Signal Line Switching Method and Apparatus*

US	Granted	14-Mar-1994	212,372	05-Sep-1995	5,448,572
JP	Granted	26-Jun-1992	168828/92	21-Nov-1996	2113094

**CaseNumber Title**

**FE-00070** Gate Overlapped Lightly Doped Drain For Buried Channel Devices

Country	Status	File Date	ApplNumb	Issue Date	PatNumber
GB	Granted	26-May-1994	94108054.1	29-Nov-1995	0684640
US	Granted	30-Apr-1993	054,994	25-Oct-1994	5,358,879
FR	Granted	26-May-1994	94108054.1	29-Nov-1995	684640
JP	Granted	04-Jun-1994	6-127422	19-Sep-1997	2698046
DE	Granted	26-May-1994	94108054.1	29-Nov-1995	0684640
EP	Granted	26-May-1994	94108054.1	10-Nov-1999	0684640

**FE-00071** Current Overload Protection Circuit

**FE-00072** Single Event Upset Hardened CMOS Latch Circuit

US	Granted	12-Jan-1995	371,718	10-Oct-1995	5,457,591
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**FE-00073** Magnification Correction For I-X Proximity X-Ray Lithography

US	Granted	01-Feb-1995	382,112	02-Apr-1996	5,504,703
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**FE-00074** Single Event Upset Immune Register With Fast Write Access

US	Granted	17-Feb-1995	309,993	02-Apr-1996	5,504,793
US	Granted	21-Feb-1995	391,798	11-Jun-1996	5,525,923

**CaseNumber Title**  
**FE-00075 Checkpoint Retry Mechanism**

Country	Status	File Date	AppNum	Issue Date	PatNumber
US	Abandon	23-Aug-1988	235,345	27-Mar-1990	4,912,707
JP	Abandon	11-Aug-1989	0207115	07-Apr-1995	1922412
GB	Abandon	08-Jun-1989	89110329.3	13-Aug-1995	0355286
DE	Abandon	08-Jun-1989	89110329.3	13-Aug-1995	0355286
FR	Abandon	08-Jun-1989	89110329.3	13-Aug-1995	0355286
EP	Abandon	08-Jun-1989	89110329.3	13-Aug-1995	0355286

**FE-00090 Efficient Dual Source Fault Tolerant Power Controller**

US	Granted	16-Nov-1995	559,584	28-Jan-1997	5,598,041
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**FE-00091 A Scaleable, Radiation Hardened Shallow Trench Isolation**

US	Abandon	01-Jul-1999	60/142,035		
US	Pending	30-Jun-2000			

**FE-00092 Apparatus And Method For Cooling Standard Electronic Modules**

US	Abandon	19-Jan-1996	588,804		
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**FE-00101 Error Detection and Fault Isolation For Lockstep Processor Systems**

US	Granted	07-Jun-1996	660,640	22-Jun-1999	5,915,082
US	Granted	04-Jun-1999	325,841	16-May-2000	6,065,135

**FE-00107 X-Ray Mask Pellicle**

US	Granted	06-Sep-1996	716,657	11-Aug-1998	5,793,836
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Tuesday, November 21, 2000

<i>CaseNumber Title</i>	<i>Country</i>	<i>Status</i>	<i>File Date</i>	<i>ApplNumb</i>	<i>Issue Date</i>	<i>PatNumber</i>
<i>FE-00113 Process To Personalize Master Slice Wafer And Fabricate High Density VLSI Components With A Single Masking Step</i>	US	Granted	10-Oct-1996	728,080	12-Jan-1999	5,858,817
<i>FE-00114 Fault Tolerant MOSFET Driver</i>						
<i>FE-00115 Lithographic Patterning Method And Mask Set Therefor With Light Field Trim Mask</i>	US	Granted	16-Oct-1996	733,080	18-Aug-1998	5,796,274
<i>FE-00121 Ring Domains For Bandwidth Sharing</i>	US	Granted	31-Oct-1996	740,598	15-Sep-1998	5,807,649
<i>FE-00122 Electrostatic Discharge Protection For Silicon-On-Insulation</i>	US	Granted	06-Mar-1997	812,184	04-May-1999	5,901,148
<i>FE-00124 Dual Mode Telephone Handset Satellite Telephone Handset -</i>	US	Granted	06-Mar-1997	812,183	07-Mar-2000	6,034,399
<i>FE-00124-1 Satellite Telephone Handset</i>	US	Granted	27-Mar-1997	29069642	28-Sep-1999	D414,486
<i>FE-00126 Secure Data Transmission on A TDM Isochronous Network</i>	US	Pending	27-Aug-1999	384,429		
	US	Granted	14-Apr-1997	837,165	19-Oct-1999	5,970,095

CaseNumber Title	Country	Status	File Date	ApplNumb	Issue Date	PatNumber
FE-00130 Improved Control Telemetry Signal Communication System For Geostationary Satellites						
FE-00131 Digital Multi-Channel Demultiplexer/Multiplexer (MCD/M) Architecture	US	Pending	27-Jun-1997	884,675		
	US	Pending	23-Dec-1999	884,675		
FE-00144 Dual Mode Collision Avoidance System	US	Pending	25-Jul-2000	625,641		
	US	Granted	27-Jun-1997	884,650	02-Feb-1999	5,867,479
	US	Granted	01-Feb-1999	241,313	18-Jul-2000	6,091,704
FE-00165 Radiation Hardened Six Transistor Random Access Memory and Memory Device	US	Abandone				
FE-00170 Enhanced TRENCH Isolation (STI) Method for Fabricating Radiation-Tolerant Integrated Circuit Devices.	US	Abandone	04-Jun-1998	090,946		
	US	Granted	05-Jun-1999	325,645	29-Aug-2000	6,111,780
	WO	Pending	04-Jun-1999	US99/12442		
FE-00172 High Accuracy Fabrication Of X-Ray Masks With Optical And E-Beam Lithography	US	Pending	30-Jun-2000	512,671		
FE-00185 Integrated Circuit Package and Method Increasing Density Of I/O Leads	US	Granted	04-Jun-1996	663,826	26-May-1998	5,756,234
	US	Pending	16-Jan-1998	007,980		

CaseNumber Title	Country	Status	File Date	ApplNumb	Issue Date	PatNumber
FE-00221 Distributed Determination of Explicit Rate in an ATM Communication System	US	Expired	03-Jun-1999	60/137,595		
	US	Expired	19-Oct-1999	60/160,302		
	US	Pending	12-May-2000	570,050		
FE-00228 Elimination of Narrow Device Width Effects In Complementary Metal Oxide Semiconductor (CMOS) Devices	US	Unfiled				
FE-00233 Reversible Keypad And Display For A Telephone Handset	US	Granted	12-Dec-1997	989,463	18-Apr-2000	6,052,606
FE-00239 Recessed Gate Process For Silicon-On-Insulator Devices	US	Abandone	04-Nov-1997	964,022		
FE-00258 Shallow Isolation Trench Forming Process For Silicon-on-Insulator Technology	US	Pending	09-Dec-1997	907,016		
FE-00275 Cold Spare and Voltage Interoperable Off-Chip Driver and Associated Methods	US	Pending	05-May-2000	566,178		
	US	Expired	02-Jun-1999	60/137,174		
FE-00276 Self Equalized Low Power Precharge Sense AMP For High Speed Memory	US	Pending	12-May-2000	570,064		
	US	Expired	10-Feb-2000	60/181,559		
	US	Expired	01-Jun-1999	60/137,224		

CaseNumber Title	Country	Status	File Date	ApplNumb	Issue Date	PatNumber
FE-00277 A Memory Device Having Reduced Power Requirements And Associated Methods	US	Pending	26-May-1999	320,227		
FE-00278 A Memory Device Having A Chip Select Speedup Feature and Associated Methods	US	Pending	26-May-1999	320,207		
FE-00279 Single Event Upset Hardened CMOS Latch Circuit With Fast Write Time	US	Abandone	07-Oct-1998	168,430		
FE-00291 Multi-Channel Overvoltage Protection Circuit	US	Granted	26-Feb-1998	030,902	03-Oct-2000	6,127,879
FE-00295 Method For Fabricating Resistors Within Semiconductor Integrated Circuit Devices	US	Pending	25-Jan-2000	491,230		
FE-00300 In Situ Proximity Gap Monitor For Lithography	US	Expired	01-Feb-1999	60/110,049		
FE-00319 Enhanced Local Oxidation of Silicon (LOCOS) Method for Fabricating Radiation-Tolerant Integrated Circuit Devices	US	Pending	10-Feb-2000	502,062		
	US	Expired	24-Sep-1999	60/155,571		
	US	Unfiled				

**CaseNumber Title**  
**FE-00320 Enhanced Single Event Upset Immune Latch Circuit**

**Country Status File Date Appl/Numb Issue Date PatNumber**

US Pending 11-Jan-2000 480,454  
 WO Pending 11-Jan-2000 US00/00557  
 US Expired 28-Jul-1999 60/145,939

**FE-00321 Method and Apparatus for Hardening A Static Random Access Memory Cell From Single Event Upsets**

US Pending 17-Nov-1999 441,941  
 DE Pending 17-Nov-1999 US99/27302  
 GB Pending 17-Nov-1999 US99/27302  
 FR Pending 17-Nov-1999 US99/27302  
 EP Pending 17-Nov-1999 US99/27302  
 US Abandone 28-May-1999 60/136,480

**FE-00324 Method For Improving Radiation Tolerance of Semiconductor Integrated Circuit Devices**

US Pending 22-Jun-2000  
 US Expired 22-Jun-1999 60/139,897

**FE-00352 Method and Apparatus for a SEU Tolerant Clock Splitter**

US Expired 30-Apr-1999 60/131,926  
 US Pending 28-Apr-2000 559,661

**FE-00354 Method and Apparatus for A Scannable Hybrid Flip Flop**

US Pending 28-Apr-2000 559,660  
 WO Pending 28-Apr-2000 US00/11348  
 US Expired 30-Apr-1999 60/132,121

**Tuesday, November 21, 2000**

**CaseNumber Title**

**FE-00371** *Pattern Density Tailoring For Etching of Advanced Lithographic Masks* **Country Status** **File Date ApplNumb** **Issue Date PatNumber**

**FE-00372** *Method and Apparatus For Evaluating A Known Good Die Using Both Wire Bond and Flip-Chip Interconnects* **US** **Pending** **07-May-1999** **307,126**

**FE-00375** *Single-Event Upset Hardened Reconfiguration Bi-Stable CMOS Latch* **US** **Pending** **28-May-1999** **321,565**

**FE-00385** *Method and Apparatus for a Voltage Responsive RESET for EEPROM*  
**WO** **Pending** **20-Jan-2000** **US00/01356**  
**US** **Pending** **24-Nov-1999** **449,723**  
**US** **Abandone** **23-Dec-1999** **60/171,589**

**FE-00387** *Low-Power CMOS Device and Logic Gates/Circuits Therewith*  
**US** **Pending** **02-May-2000** **563,197**  
**US** **Expired** **02-Jun-1999** **60/137,739**

**WO** **Pending** **22-Jun-2000** **US00/11887**  
**US** **Expired** **09-Nov-1999** **60/164,343**  
**US** **Expired** **23-Jun-1999** **60/140,361**  
**US** **Pending** **21-Jun-2000** **598,681**

**Tuesday, November 21, 2000**

<i>CaseNumber Title</i>	<i>Country</i>	<i>Status</i>	<i>File Date</i>	<i>ApplNumb</i>	<i>Issue Date</i>	<i>PatNumber</i>
<i>FE-00391 Single Event Upset (SEU) Hardened Static Random Access Memory Cell</i>						
	US	Expired	28-May-1999	60/136,479		
	US	Pending	17-Nov-1999	441,942		
	US	Pending	30-Aug-2000	651,155		
	EP	Pending	17-Nov-1999	US99/27301		
<i>FE-00397 Circuit and Method For Limiting Inrush Current Through A Mosfet</i>						
<i>Circuit and Method For Limiting Inrush Current Through A Transistor/102</i>						
	US	Expired	30-Dec-1999	60/174,059		
	WO	Unfiled				
	US	Pending	12-Jun-2000	591,958		
<i>FE-00398 Integrated Resistor Having Aligned Body and Contact and Method for Forming The Same</i>						
	US	Provision	21-Jan-2000	60/170,247		
<i>FE-00406 Storage Unit Subassembly Insertion/Extraction Tool</i>						
	US	Expired	17-Feb-1999	60/120,320		
<i>FE-00410 Computer Device Having Multiple Linked Parallel Busses and Associated Method</i>						
	US	Pending	14-Sep-2000			
<i>FE-00414 Self-Restoring Single Event Upset (SEU) Hardened Multiport Memory Cell</i>						
	US	Expired	28-May-1999	60/136,478		
	WO	Pending	15-May-2000	US00/13095		
	US	Pending	20-Apr-2000	553,595		

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<i>CaseNumber Title</i>	<i>Country</i>	<i>Status</i>	<i>File Date</i>	<i>ApplNumb</i>	<i>Issue Date</i>	<i>PatNumber</i>
<i>FE-00422 System and Method of Providing a Spread Spectrum Pulse Width Modulator Clock</i>						
	US	Expired	18-Oct-1999	60/159,974		
	WO	Pending	12-Jun-2000	US00/28748		
	US	Pending	12-Jun-2000	591,731		
<i>FE-00424 Multiplexor Having A Single Event Upset (SEU) Immune Data Keeper Circuit</i>						
	US	Pending	08-Jun-2000	589,732		
<i>FE-00426 Oscillator and Method For Generating A Frequency Within A Stable Frequency Range</i>						
	US	Provision	05-Nov-1999	60/163,757		
<i>FE-00431 Method For Testing Known Good Die</i>						
	US	Pending	24-Jul-2000	624,247		
	US	Expired	25-Oct-1999	60/161,418		
<i>FE-00432 Method and Apparatus for a Single Event Upset (SEU) Tolerant Clock Splitter</i>						
	US	Expired	30-Apr-1999	60/131,925		
	WO	Pending	28-Apr-2000	US00/11349		
	US	Pending	20-Apr-2000	559,659		
<i>FE-00434 Tool Suite for the Rapid Development of Advanced Standard Cell Libraries</i>						
	US	Pending	20-Jun-2000	597,229		
<i>FE-00436 A Process For Removing A Silicon-Containing Material Through Use Of A Byproduct Generated During Formation Of A Diffusion Barrier Layer</i>						
	US	Unfiled				

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CaseNumber Title	Country	Status	File Date	App/Numb	Issue Date	PatNumber
FE-00439 Increasing The Susceptability Of Integrated Circuits To Ionizing Radiation	US	Expired	11-Jun-1999	60/138,718		
FE-00442 Semiconductor Circuit Having Increased Susceptibility To Ionizing Radiation	US	Pending	09-Jun-2000	590,805		
FE-00443 Semiconductor Device And Circuit Having Low Tolerance To Ionizing Radiation	US	Pending	09-Jun-2000	592,413		
	US	Expired	11-Jun-1999	60/138,720		
FE-00444 Apparatus And Method For Manufacturing A Semiconductor Circuit	US	Pending	09-Jun-2000	590,806		
	US	Expired	11-Jun-1999	60/138,721		
FE-00449 Method to Harden Shallow Trench Isolation Against Total Ionizing Dose Radiation	US	Pending	09-Jun-2000	590,809		
FE-00450 A New Radiation-Hardened Technique For Preventing Latches From Single Event Upsets	US	Pending	31-Jul-2000			
	US	Expired	02-Aug-1999	60/146,895		
FE-00451 Radiation Hardened High Speed Differential Driver	US	Provided	11-Aug-2000	60/224,649		
	US	Expired	20-Jul-1999	60/144,731		

CaseNumber Title	Country	Status	File Date	App/Num	Issue Date	PatNumber
FE-00453 Radiation Hardened High Speed Differential Receiver	US	Expired	20-Jul-1999	60/144,625		
FE-00456 Radiation Hardened Silicon-On-Insulator (SOI) Transistor Having A Body Contact	US	Pending	01-Aug-2000	630,216		
FE-00458 Circuit For Filtering Single Event Effect (SEE) Induced Glitches	US	Expired	23-Dec-1999	60/171,569		
FE-00462 Method and Apparatus Radiation Hardened Clock Splitter	US	Pending	30-Aug-2000	651,156		
	US	Expired	07-Sep-1999	60/152,348		
	WO	Pending	06-Sep-2000	US00/24421		
FE-00464 Single Event Upset Immune Oscillator Circuit	US	Provision	28-Apr-2000	60/200,348		
FE-00469 Redundant Oscillator and Method For Generating A Regulated Signal	US	Pending	21-Sep-2000	667,040		
FE-00470 Controlled Hermetic Solder Sealing For Large Perimeter Components	US	Pending	10-Aug-2000	636,125		
	US	Abandoned	20-Jan-2000	60/177,234		
	US	Expired	18-Jan-2000	60/176,574		

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CaseNumber Title	Country	Status	File Date	App/Num	Issue Date	PatNumber
FE-00471 Integrated Circuits Containing Transistors Operable With Two Power Supply Voltages						
FE-00475 Voltage Step-Up Output Buffer With Low Stress	US	Unfiled				
	US	Provided	11-Aug-2000	60/224,650		
FE-00476 Structured Login After Satellite Service Interruption	US	Expired	30-May-2000	60/207,913		
FE-00480 Self-Oscillating Switching Regulator	US	Expired	18-Jan-2000	60/176,606		
FE-00481 A Radiation Tolerant Storage Array Sense Latch	US	Pending	03-Oct-2000			
FE-00483 Polyphase-DFT Sub-band Definition Filtering Architecture	US	Provided	11-Aug-2000	60/224,648		
FE-00486 Use of Chalcogenide For Programming Fuses In RAM's or Other Devices	US	Provision	11-Feb-2000	60/181,512		
FE-00489 Direct Chip Attach Micro-CGA	US	Provision	02-May-2000	60/201,122		
	US	Unfiled				

<i>CaseNumber Title</i>	<i>Country</i>	<i>Status</i>	<i>File Date</i>	<i>ApplNumb</i>	<i>Issue Date</i>	<i>PatNumber</i>
FE-00491 <i>Rad Hard Ring Oscillator</i>						
FE-00492 <i>Single Event Upset Immune Logic Family</i>	US	Unfiled				
			12-May-2000	60/203,895		
FE-00498 <i>A Sense Amp Scheme Hardened for Dynamic Single Event Upsets</i>	US	Provision				
	US	Unfiled				
FE-00503 <i>Remote Pictures</i>	US	Provision	06-Jun-2000	60/209,665		
FE-00505 <i>Reduced Stress Interface Column Grid Array</i>	US	Unfiled				
FE-00508 <i>Remote Sonar Buoys</i>	US	Unfiled				
FE-00512 <i>Method For Advanced Fill Pattern Creation</i>	US	Unfiled				
FE-00513 <i>Power Conservation Circuit Using The "Seebeck" Effect</i>	US	Unfiled				

CaseNumber Title	Country	Status	File Date	ApplNumb	Issue Date	PatNumber
FE-00515 Method Of Forming and Applications of Micropipes and Chalcogenide Waveguides						

FE-00516 Fault Isolation Test Methodology	US	Unfiled				
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FE-00521 Novel High-Density High-Performance CMOS SRAM Cell Design	US	Unfiled				
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FE-00522 Novel CMOS SRAM Cell Design with Prescribed Power-On Data State	US	Unfiled				
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	Pending	25-Jul-2000	60/220,700			
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FE-00527 Solder Column Attach						
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FE-00527 On-Chip High Speed Termination						
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FE-00528 An Institute Radiation Action of Integrated Circuits						
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FE-00539 Visitor Information System (VIS)						
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FE-00540 Small Area Sidewall Rapier Contact For Chalcogenide Memory Device						
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FE-00542 EGA to CGA Conversion Process						
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